AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-21 (Cancelled)

22. (Currently Amended) A method for driving a plurality of pixels in a display panel by a display driver in accordance with a positive phase and a negative phase of a display mode, the method comprising:

inputting display data to a first driver in the display driver;

converting the display data into first display data in the positive phase and into second display data in the negative phase using a converting circuit in the display driver in response to a switching signal in synchronization with switching between the positive phase and the negative phase,

the converting of the display data being performed such that one specified bit of the display data is set to logic "0" by a first exclusive logic circuit when the switching signal and the one specified bit match each other and is set to logic "1" by the first exclusive logic circuit when the switching signal and the one specified bit do not match each

other, and such that each of other bits of the display data is set to logic "1" by an associated second exclusive logic circuit of a plurality of second exclusive logic circuits when the one specified bit matches the other bit and set to logic "0" by the associated second exclusive logic circuit when the one specified bit does not match the other bit, ~~so that~~ whereby the first display data and the second display data are in the same bit pattern except for the one specified bit when converting the display data;

generating a plurality of gradation voltages using a gradation voltage generating circuit in the display driver;

generating a first common voltage in the positive phase and a second common voltage, different from the first common voltage, in the negative phase using a common voltage driver in the display driver, wherein the first and the second common voltage is applied to a common electrode of the plurality of pixels in the display panel;

selecting, using a selector in the display driver, a first gradation voltage from the plurality of gradation voltages based on the first display data in the positive phase and a second gradation voltage from the plurality of gradation voltages based on the second display data in the negative phase, wherein the first and the second gradation

voltages are applied to a pixel electrode of a selected pixel of the plurality of pixels in the display panel;

in the positive phase, providing the first gradation voltage and the first common voltage to the display panel; and

in the negative phase, providing the second gradation voltage and the second common voltage to the display panel.

23. (Previously Presented) A method according to claim 22, wherein the one specified bit is the highest order bit.

Claim 24 (Cancelled)

25. (Previously Presented) A method according to claim 22,

wherein the display driver further comprises a RAM, and

wherein, in said inputting, the display data is provided from the RAM to the first driver.

26. (Previously Presented) A method according to claim 22, wherein, in said inputting, the display data is provided from a microcomputer.

27. (Currently Amended) A display system comprising:

a display panel including a plurality of signal lines, a plurality of scanning lines, a common electrode, a plurality of pixels coupled to the plurality of signal

lines, the plurality of scanning lines, and the common electrode so that one pixel is coupled to one signal line, one scanning line, and the common electrode, wherein one pixel includes a MOSFET having a gate coupled to one scanning line and a source-drain path coupled between one signal line and a pixel electrode opposite to the common electrode;

a display driver coupled to the plurality of signal lines, the plurality of scanning lines, and the common electrode, wherein the display driver comprises:

a gradation voltage generator providing a plurality of gradation voltages;

a first driver coupled to the plurality of signal lines and including:

a converting circuit coupled to receive display data and responsive to a switching signal which controls a switching of a positive phase and a negative phase, and which provides first data in the positive phase and second data in the negative phase, such that one specified bit of the display data is set to logic "0" by a first exclusive logic circuit when the switching signal and the one specified bit match each other and is set to logic "1" by the first exclusive logic circuit when the switching signal and the one specified bit do not match each other, and such

that each of other bits of the display data is set to logic "1" by an associated second exclusive logic circuit of a plurality of second exclusive logic circuits when the one specified bit matches the other bit and set to logic "0" by the associated second exclusive logic circuit when the one specified bit does not match the other bit, whereby ~~so that~~ the first data and the second data are in the same bit pattern except for the one specified bit when converting the display data, and

selectors coupled to receive the plurality of gradation voltages and to select ones of the plurality of gradation voltages for the plurality of signal lines, respectively, in response to the first and the second data;

a second driver coupled to the plurality of scanning lines and which outputs a selection signal to sequentially select one of the plurality of scanning lines; and

a third driver coupled to the common electrode and which provides, to the common electrode, a first common voltage in the positive phase and which provides, to the common electrode, a second common voltage different from the first common voltage in the negative phase.

28. (Previously Presented) A display system according to claim 27, wherein the one specified bit is the highest order bit.

Claim 29 (Cancelled)

30. (Currently Amended) A display system according to claim [[29]]28, wherein the display driver further comprises a display memory which provides the display data.

31. (Previously Presented) A display system according to claim 30, wherein the display driver is on a semiconductor substrate.

32. (Previously Presented) A display system according to claim 27, wherein the display driver is on a semiconductor substrate.

33. (Previously Presented) A display system according to claim 27, further comprising a microcomputer which provides the display data.

34. (Currently Amended) A display driver on a semiconductor substrate and for use with a display panel including a plurality of signal lines, a plurality of scanning lines, a common electrode, a plurality of pixels coupled to the plurality of signal lines, the plurality of scanning lines, and the common electrode so that one pixel is coupled to one signal line, one scanning line, and the common electrode, wherein one pixel includes a MOSFET having a gate coupled to one scanning line and a source-drain path

coupled between one signal line and a pixel electrode opposite to the common electrode, and wherein the display driver is coupled to the plurality of signal lines, the plurality of scanning lines, and the common electrode, the display driver comprising:

a gradation voltage generator which provides a plurality of gradation voltages;

a display memory which stores display data;

a first driver to be coupled to the plurality of signal lines and including:

a converting circuit coupled to receive the display data, and which is responsive to a switching signal that controls a switching of a positive phase and a negative phase, and which provides first data in the positive phase and second data in the negative phase, such that one specified bit of the display data is set to logic "0" by a first exclusive logic circuit when the switching signal and the one specified bit match each other and is set to logic "1" by the first exclusive logic circuit when the switching signal and the one specified bit do not match each other, and such that each of other bits of the display data is set to logic "1" by an associated second exclusive logic circuit of a plurality of second exclusive logic circuits when the one specified bit matches the other bit and set to logic "0"

by the associated second exclusive logic circuit when the one specified bit and does not match the other bit, whereby~~so that~~ the first data and the second data are in the same bit pattern except for the one specified bit when converting the display data, and

selectors coupled to receive the plurality of gradation voltages, and which select ones of the plurality of gradation voltages for the plurality of signal lines, respectively, in response to the first and the second data;

a second driver coupled to the plurality of scanning lines, and which outputs a selection signal to sequentially select one of the plurality of scanning lines; and

a third driver coupled to the common electrode, and which is provides to the common electrode a first common voltage in the positive phase and which provides to the common electrode a second common voltage different from the first common voltage in the negative phase.

35. (Previously Presented) A display driver according to claim 34, wherein the one specified bit is the highest order bit.

Claim 36 (Cancelled)